WHAT IS CLAIMED IS:

1. An apparatus for generating PN(pseudo noise) codes comprising:

a control unit for outputting a control signal for the normal state or a PN chip advance;

a plurality of MUXs for outputting an output value of the next state for normal operation or an output value of a PN chip advance as an output signal in response to the control signal of said control unit;

a plurality of shift registers connected for outputting PN chip codes of the next or the second next state during one system clock time period in response to said MUXs, the input end of each of said shift registers being connected to the output end of each of said MUXs.

2. The apparatus for generating PN codes according to claim 1, wherein said control unit further outputs a control signal for a PN chip retard; and wherein said MUXs further outputs a value for said PN chip retard.

3. A method for generating PN codes in an n stage PN code generator comprising an LSSR(linear sequence shift register) including n number of shift registers connected in series and n number of MUXs, the output end of each of the n number of MUXs being connected to input end of said n shift registers, said method comprising the steps of:

inputting signals to perform an operation for obtaining the next state of the LSSR in the normal state and an operation for obtaining the next state of the LSSR for a PN chip advance into each of the n MUXs;

generating the control signals for changing the next state in respect to the LSSR;

multiplying signals input to each of the MUXs in response to the control signals; and

performing an operation corresponding to the multiplied signals during one clock.

4. The method for generating PN codes according to claim 3, wherein said operation for obtaining the next state of the LSSR for the PN chip advance comprises:

inputting a resultant value of OR operating an output signal of (n-1)th shift register and a resultant value of AND operating an output signal of nth shift register and (n-1)th value of generation polynomial given to the PN code generator into an input end of first shift register of the n number of shift registers; and

inputting a resultant value of OR operating first, second and third values at the same time into the input end of random ith shift register except the first shift register, the first value being obtained from OR operating an output signal of (i-1)th shift register of generation polynomial and a resultant value of OR operating an output signal of the (n-1)th shift register and a resultant value of AND operating an output signal of the nth shift register and (n-1)th value of the generation polynomial, the second value being obtained from AND operating an output signal of the nth shift register and (i-2)th value of the generation polynomial, and the third value being an output signal of (i-2)th retard device.

5. The method for generating PN codes according to claim 3, wherein an operation for the PN chip retard for the LSSR is performed to disable external enable signals applied to each of the shift registers during one PN chip time period.

6. The method for generating PN codes according to claim 4, wherein if the generation polynomial is nth order generation polynomial g(X) and the nth order generation polynomial g(X) is

$$g(X) = g_n X^n + g_{n-1} X^{n-1} + \ldots\ldots + g_1 X + 1 \ ,$$

the nth order generation polynomial g(X) is

$$\vec{g} = [g_n \quad g_{n-1} \quad \ldots\ldots \quad g_1 \quad g_0] \ ,$$

$$g_i = \begin{cases} 1 & ,i = n \\ 0 \text{ or } 1 & ,0 < i < n, \quad \textit{wherein } i \textit{ is an integer} \\ 1 & ,i = 0 \end{cases}$$

7. The method for generating PN codes according to claim 6, wherein if the present state of the LSSR is assumed $\vec{r}_m$, and the present state of the LSSR is expressed as

$$\vec{r}_m = \left[r_{n,m} \quad r_{n-1,m} \quad \ldots\ldots \quad r_{1,m} \quad r_{0,m} \right]$$

$$r_{i,m} = \begin{cases} 0 \text{ or } 1 & ,0 < i \le n, \ \textit{wherein } i \textit{ is an integer} \\ 0 & ,i = 0 \end{cases}$$

, and the PN code generator is normally operated, the next state $\vec{r}_{m+1}$ of the LSSR according to the present state $\vec{r}_m$ of the LSSR, MSB(most significant bit) $r_{n,m}$ and generation polynomial $\vec{g}$ is

$$\vec{r}_{m+1} = \lfloor r_{n,m} \; r_{n-1,m} \; \cdots\cdots \; r_{1,m} \; r_{0,m} \rfloor \; ,$$

$$r_{i,m+1} = \begin{cases} r_{i-1,m} \oplus (r_{n,m} g_{i-1}), 0 < i \le n, \; wherein \; i \; is \; an \; integer \\ 0 \qquad\qquad\qquad\qquad , i = 0 \end{cases}$$

8. The method for generating PN codes according to claim 6, wherein the second next state $\vec{r}_{m+2}$ of the LSSR for performing one PN chip advance of the LSSR according to the present state $\vec{r}_m$ of the LSSR and nth generation polynomial $\vec{g}$ is

$$\vec{r}_{m+2} = \lfloor r_{n,m+2} \; r_{n-1,m+2} \; \cdots\cdots \; r_{1,m+2} \; 0 \rfloor \; ,$$

$$r_{i,m+2} = \begin{cases} r_{i-2,m} \oplus (r_{n,m} g_{i-2}) \oplus [\{r_{n-1,m} \oplus (r_{n,m} g_{n-1})\} g_{i-1}], 1 < i \le n, \; wherein \; i \; is \; an \; integer \\ r_{n-1,m} \oplus (r_{n,m} g_{n-1}) \qquad\qquad\qquad\qquad , i = 1 \\ 0 \qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad , i = 0 \end{cases}$$

9. The method for generating PN codes according to claim 3, further comprising inputting a signal for performing an operation to obtain the next state of the LSSR for the PN chip retard to each of the n MUXs.

10. The method for generating PN codes according to claim 9, wherein said operation for

obtaining the next state of the LSSR for the PN chip retard causes feedback of an output signal of the ith shift register to the input end of the ith shift register, or disables an external signal applied to each shift register during one PN chip time period.

11. An apparatus for generating PN codes comprising:

first circuit for obtaining the next normal state of n bit length shift registers;

second circuit for obtaining the next state of shift registers for one PN chip advance;

third circuit for obtaining the next state of the shift registers for one chip retard; and

n number of MUXs arranged in the input end of each of the shift registers.

12. The apparatus for generating PN codes according to claim 11, wherein said first circuit is adapted to connect output signals of each of the shift registers into the input ends of the shift registers connected to the output ends of said MUXs via said MUXs;

wherein said second circuit is adapted to input an output signal of nth shift register to first shift register of the n bit length shift registers, and to input an output signal of the ((i-2))th shift register to the input end of random ith shift register except the first shift register; and

wherein said third circuit is adapted to input an output signal in each of the shift registers into one input end of said MUXs, the output end of each of said MUXs being connected to the input end of each of the shift registers.

13. The apparatus for generating PN codes according to claim 11, further comprising a plurality

of comparators for comparing the present load state and the next load state of each of the shift register outputs.

14. The apparatus for generating PN codes according to claim 11, further comprising a MUX for outputting compared values of the present load state and the next load state of the shift registers, and load commands of each of the shift registers from the one PN chip advance commands or the one PN chip retard commands.

15. The apparatus for generating PN codes according to claim 11, further comprising a decoder for generating a control signal for controlling said MUX from the one PN chip advance or one chip retard inputs.

16. An apparatus for generating PN codes comprising:

n number of first MUX group;

n number of LSSRs having input ends connected to said n number of first MUX group;

first and second comparators for comparing the present load state and the next load state of said n number of LSSRs;

second MUX for receiving an externally applied advance or retard signal and the signals from said comparators to output one selected from group including the next state, the second next state and the present state signals;

a combinational circuit for receiving and combining the output signal of said second MUX,

the externally applied advance or retard signal and a compared output signal from said first and second comparators to output the resultant combined values; and

a decoder for outputting the output resultant value from said combinational circuit into each of said n number of first MUX group during one system clock.